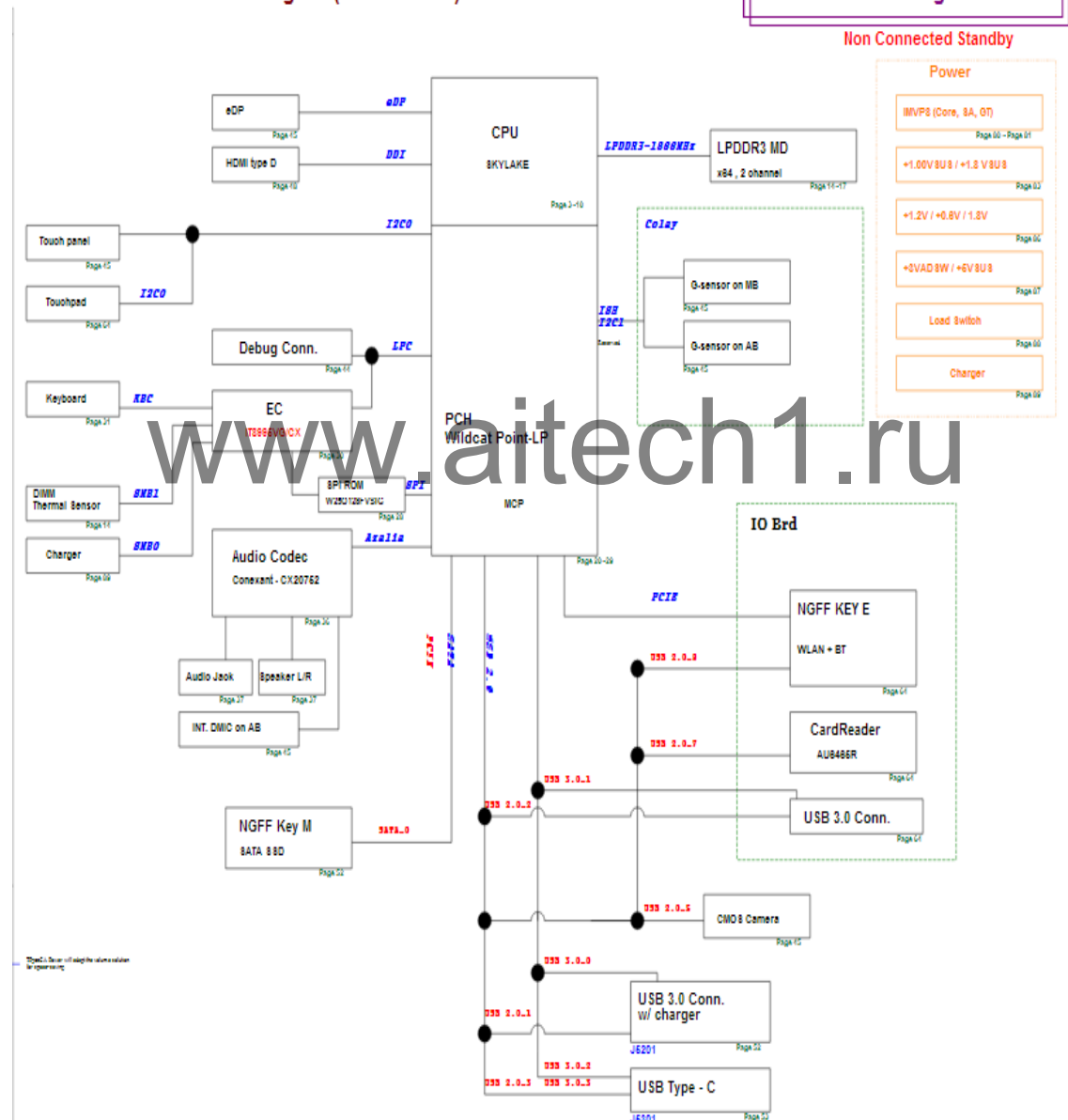
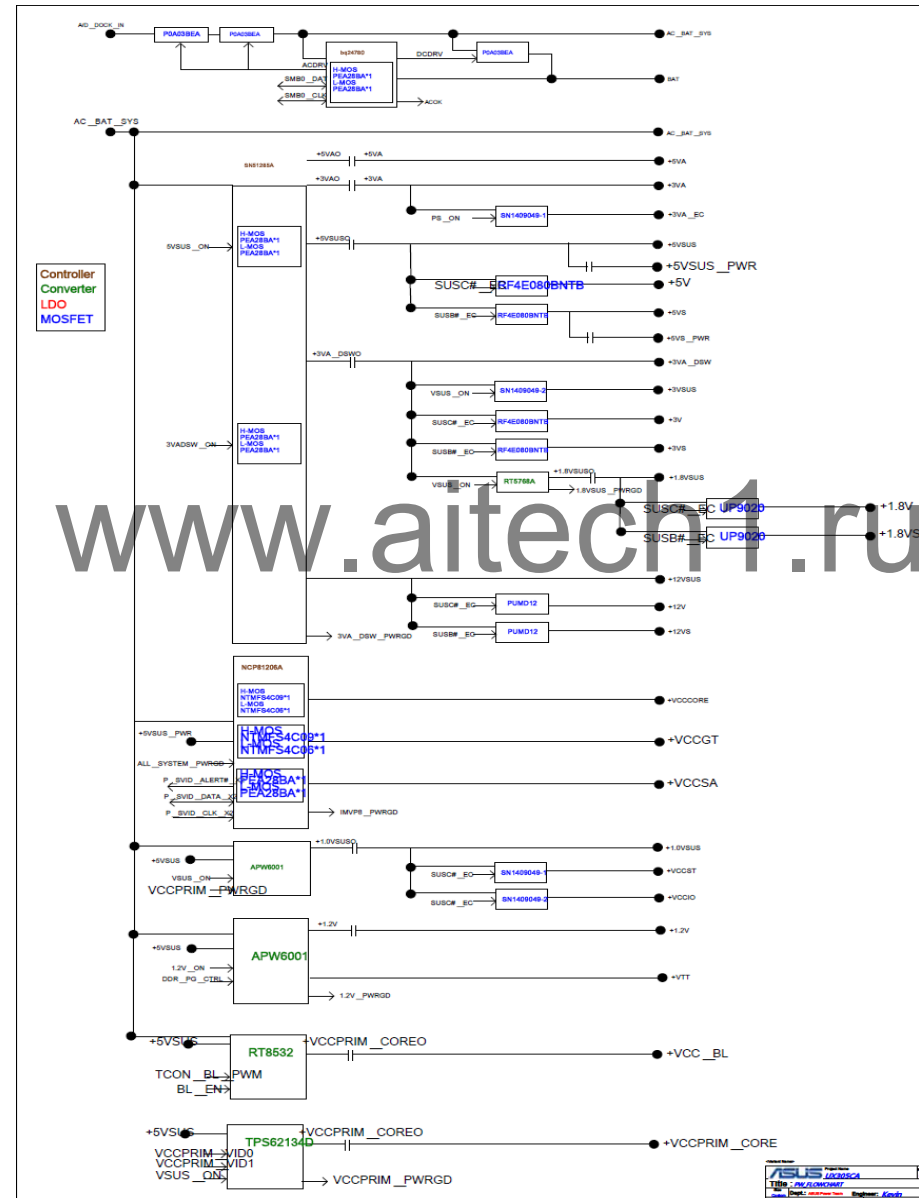


UX360CA Block Diagram (Y-Processor) Ver. 2.0

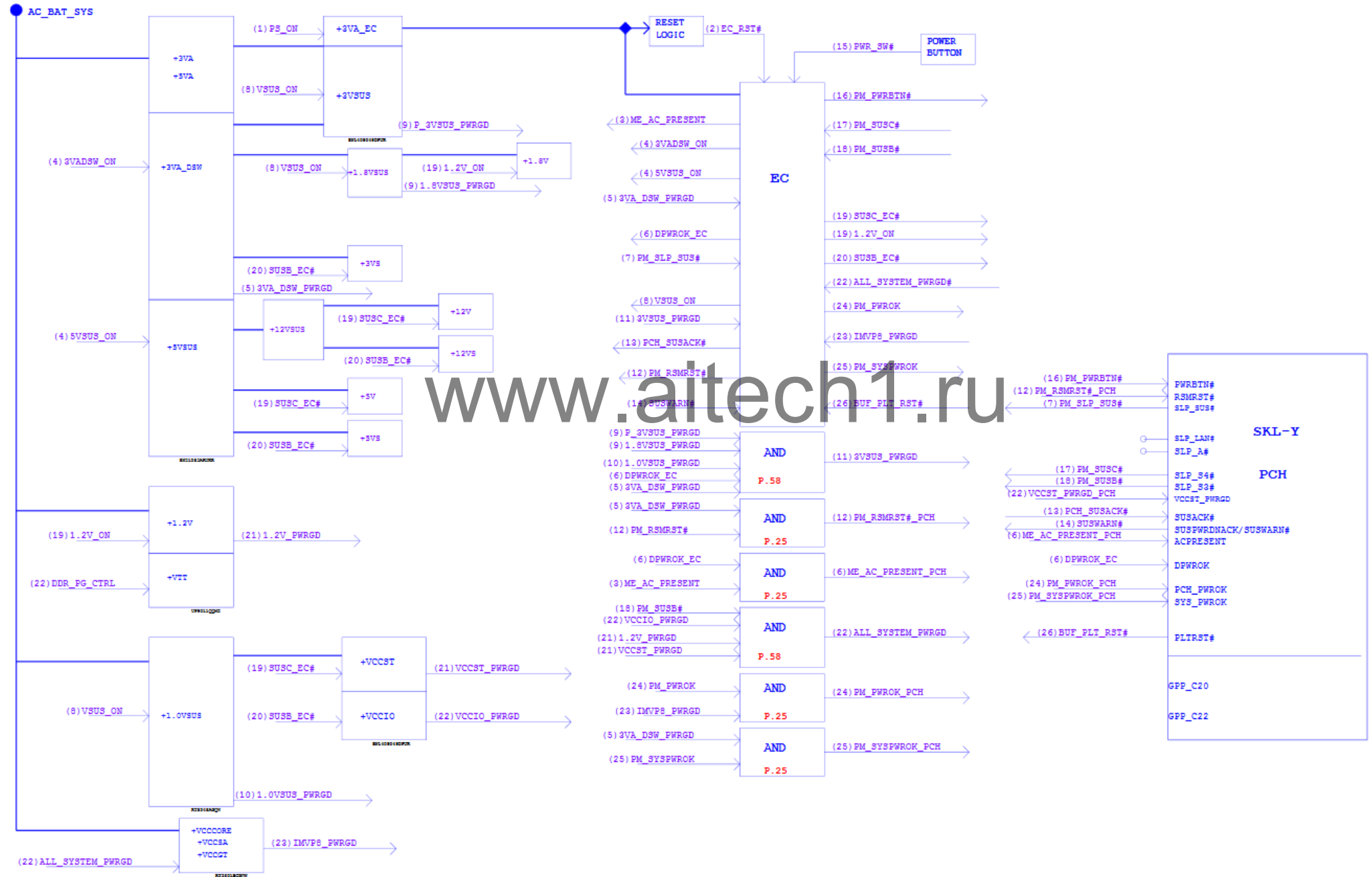


POWER FLOW



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Power On Sequence Diagram Rev.1.0



AC POWER ON SEQUENCE

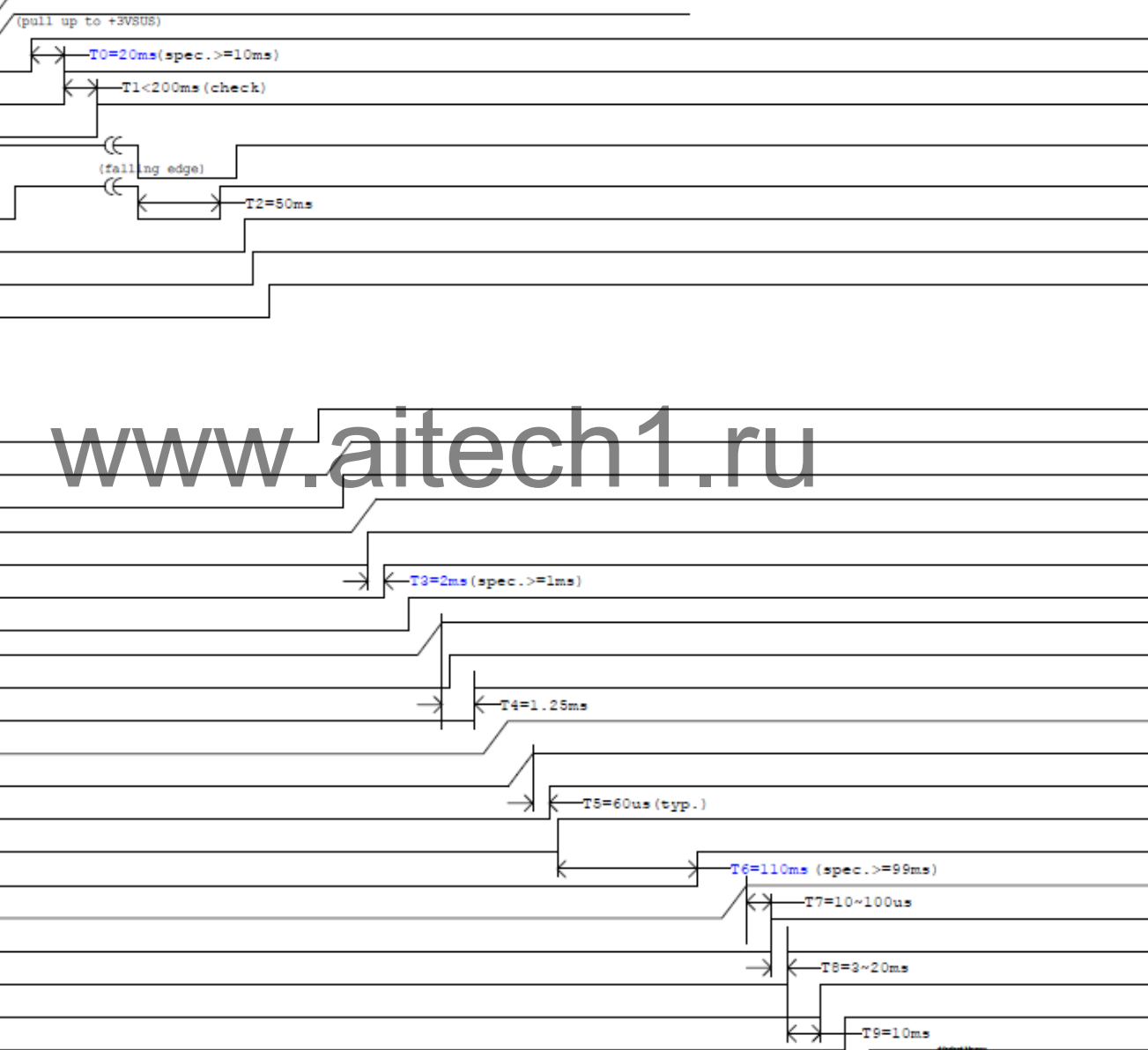
AC-IN Mode

1 +3VA/+5VAO/+3VA_EC
(to EC) 2 EC_RST#
(EC to power) 3 VSUS_ON
+3VSUS/+5VSUS
(PCH to EC) 4 ME_SusPwrDnAck_R
(power to EC) 5 3VSUS_PWRGD
(EC to PCH) 6 PM_RSMRST#
(EC to PCH) 7 ME_AC_PRESENT
(to EC) 8 PWR_SW#
(EC to PCH) 9 PM_PWRBTN#
(PCH to EC) 10 PM_SLP_A_R#
(PCH to EC) 11 PM_SUSC#
12 PM_SUSB#/SLP_LAN#
(PCH to EC) (PCH to power)

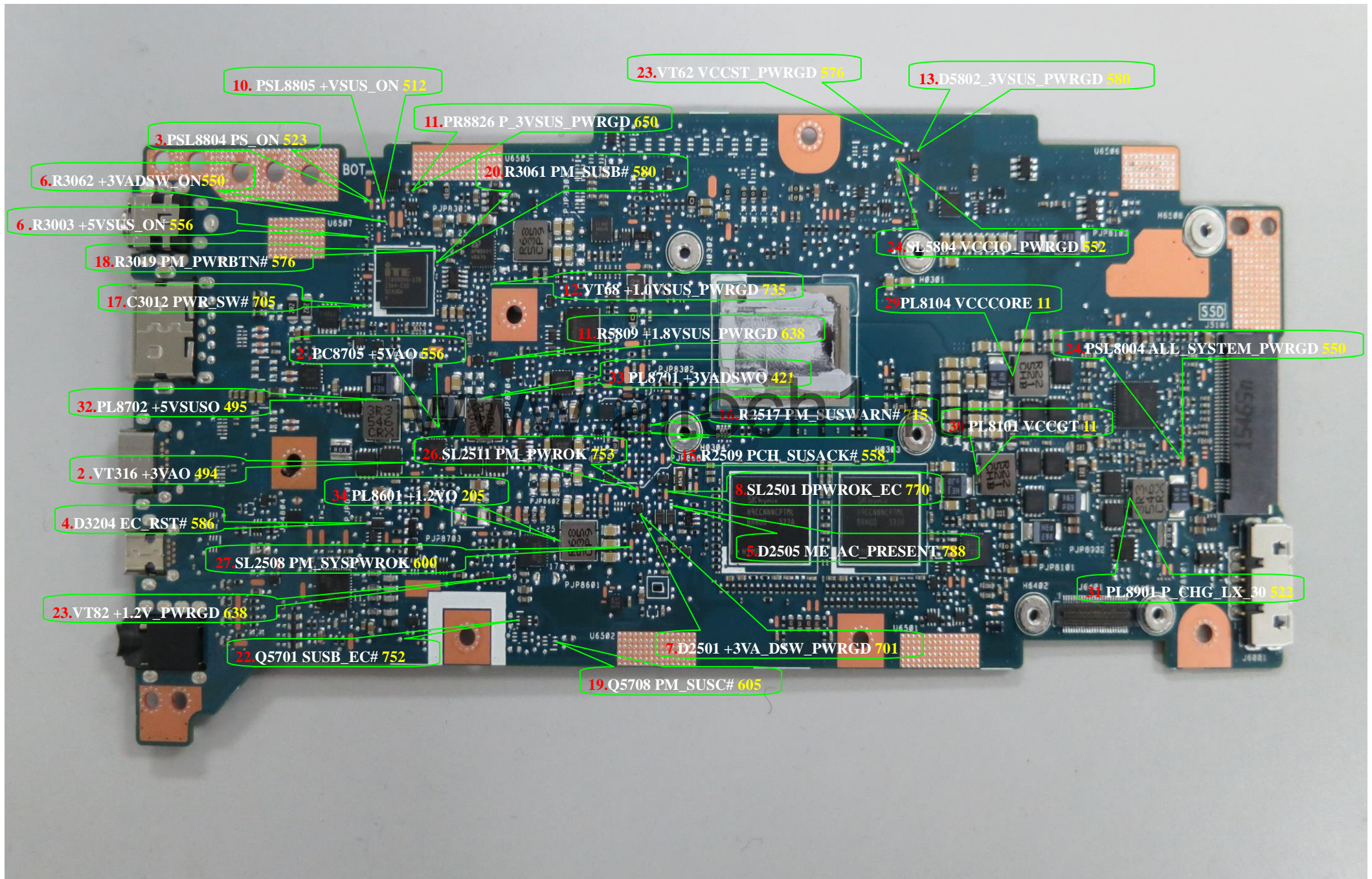
(EC to power) 13 SUSC_EC#
+0.6V/+1.2V/+1.8V/+3V/+5V
(EC to power) 14 SUSB_EC#
+1.8VS/+3VS/+5VS
(power to EC) ME_VM_PWRGD
(EC to PCH) ME_PWROK
15 SYSTEM_PWRGD
+VTT_CPU
(CPU to power) GFX_VR_ON
16 +VTT_CPU_PWRGD/ 17 H_VITPWRGD
(power to CPU)
GFX_VID
+VGFX_CORE
(power to EC) GFX_PWRGD
18 ALL_SYSTEM_PWRGD
(EC to power) CPU_VRON
19 +VCCIN
CLK_PWRGD
(inversion of CLK_EN#)
(power to EC) 20 CORE_PWRGD
(EC to PCH) 21 PM_PWROK
(PCH to CPU) H_DRAM_PWRGD
(PCH to CPU) H_CPUPWRGD
(PCH to CPU) 22 BUF_PLT_RST#

T300CA Power-On Sequence Timing Diagram Rev.0.1

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Signal Measure Point-Bottom



Signal Measure Point-Top

